**General Design Guidelines**

**General**

* Trace to trace spacing digital to digital – 5H and at least 3H if you get space issues.
* Trace to Trace spacing - digital to RF – use 20H separation between RF and digital signals and at least 10H if you get space issues.
* Do not split RF and digital grounds to avoid EMI issues, just keep the 20H separation rule above.

**Power and Decupling**

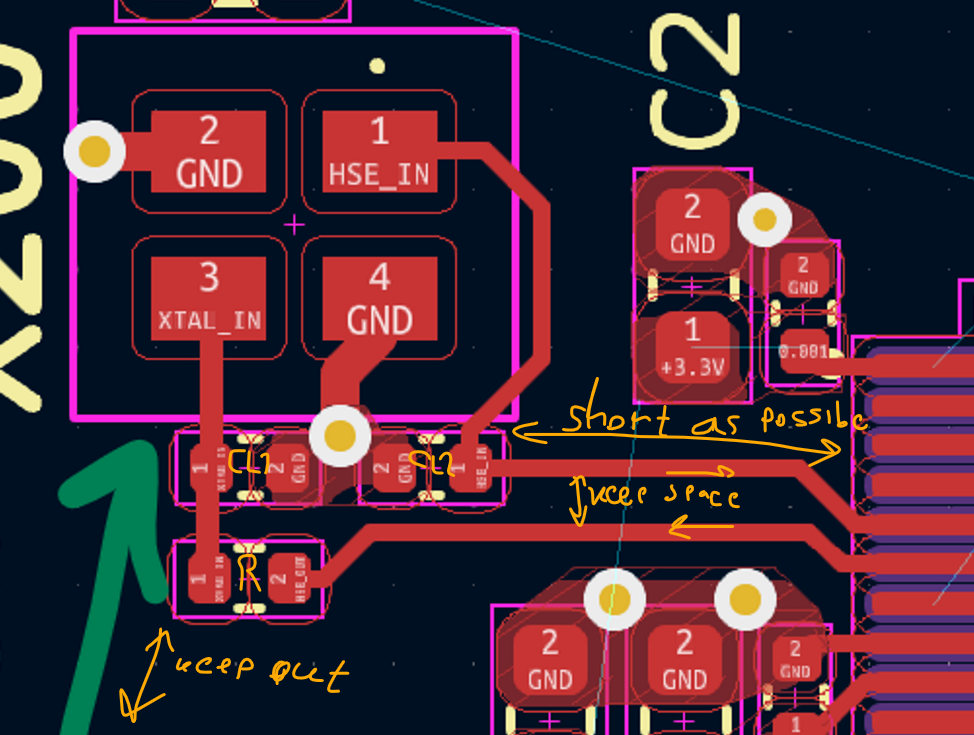
* Place small decupling first close to the power pin, then medium size and then bulk capacitors.
* **Power traces/polygons** - Route the power pins with polygons to the capacitors as wide as possible and min power trace width of **0.3mm trace** -> 1.7[mOhm/mm] -> 1A ([PCB Trace width Calculator](https://www.4pcb.com/trace-width-calculator.html))
* **LDO** **Power traces** should be able to provide 2A bursts so keep power traces from the LDO with wide polygons and minimum power trace of **1mm trace** -> 0.8[mOhm/mm] -> 2A ([PCB Trace width Calculator](https://www.4pcb.com/trace-width-calculator.html))
* PIMIC/LDO input/output caps with small loops and close to the BUCK
* Use reference/stitching vias close to the POWER VIAS
* Keep small loops connection (vias placement tight)
* Keep feedback lines of the buck and the PIMIC away from circuitry.
* Add as many GND vias as possible for better EMI and heat dissipation.
* Switch note only as large as needed for current – (Keep the connection from the buck to the inductor wide enough for the current requirement but not more than that)**. (max width calculation needed here)**
* Place ESD TVS diods as close as possible to the USB connectors.
* **PowerGood and Enable signals are less critical and route it last(before stitching vias)**
* **Power vias**: vias comes in pairs, move vias closer to reduce inductance for smaller loops.
* Split the power plane 4 to the zync voltages.
* Use L8 power polygons for the GSM Power
* Use chassis capacitor and connect all external connectors to the chassis capacitor.

**Zync Routing**

Use “dog-bone” method and fit the trace width dog bone as required for the controlled impedance traces (use the width from the width table)

**XTAL** - **critical line**

* Placement with no stubs of CL1/2 and R – see example below.
* Keep away from other High speed or PWM signals.
* Keep space as possible from the consumer input and outputs.
* Keep out from other high speed or critical lines.
* Note this design guide document: [XTAL Design guidelines by ABARCON](https://abracon.com/Support/appendix-a.pdf)
* Example for XTAL layout and routing:



**CMOS Oscillator Layout and Routing – Critical line**

* + Place OSC as close as possible to its consumer and in the resistor.
  + Resistor right after and then short trace to the consumer
  + Place it in a way that with his resistor there are no stubs.
  + Decup oscillator below with short loops
  + Oscillator Layout Layout example:



**EEPROM Layout and Routing**

* The EEPROM is not very fast but still try to keep traces short.
* Option to place it in the bottom Layer and then:
  + Decupling close with short loops
  + Pull ups close.
* Example from previous project:

A screenshot of a computer

Description automatically generatedA computer screen shot of a circuit board

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**EMMC layout and routing (0.5mm pitch)**

* See the attached document “[Recommended\_PCB\_Routing\_Guidelines\_for\_SHM\_e.MMC.pdf](http://www.skyhighmemory.com/download/applicationNotes/Recommended_PCB_Routing_Guidelines_for_SHM_e.MMC.pdf)”
* EMMC is with 0.5mm pitch but most of the pins are NC so can “de-populate” unused pins
* Placement close, up-right to the Zynq(SDIO pins there in upper-left)
* Terminations (pull ups) at the top layer near the EMMC
* Route SDIO traces:
  + to Layer 6 (good for high speed)
  + 50 ohm controlled impedance
  + Traces lengths as short as possible (about 30ps??)
  + Keep spacing between traces - more than the manufacturer limit(as possible)

For example:

**A screenshot of a computer program

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**Boot parts guidelines:**

* QSPI Routing:
  + Data lines delay matching
  + QSPI CLK, a bit longer then the QSPI Data lines(and not shorter)
* JTAG Pins as 50 ohms (optional at layer 6 if there is enough space)
* Placement:
  + Place dip switch on the bottom (trough hole VIA) to avoid stubs
  + Place dip switch resistors (3 pull ups and 3 pull downs) near the dip switch on the bottom
  + Place the JTAG header(not used in this project) above the DIP switch on the TOP(avoid stubs)

**Differential lines**

* More important so first - Intra – pair skew - P to N matching (same diff channel)
* Then - Inter pair skew matching (diff to diff)

**GSM part**

* Placement on the bottom and route to the power planes on layer
* Keep spacing of 20H of RF signals(GSM and muRata) to digital signals
* Use the placement recommendation drawing in the [SARA-G450 - System integration manual](https://content.u-blox.com/sites/default/files/SARA-G450_SysIntegrManual_UBX-18046432.pdf) for example:

A diagram of a circuit

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A screenshot of a computer scheme

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**DDR3L Memory:**

* DDR Routing – Zync - > DDR3L -> VTT Resistors -> bypass capacitors
* Route clock signals first
* DDR3 DQ/DM to DQS\_P/N skew limit is **50ps** maximum but keep as low as possible.
* DDR3 Address to Clock Skew Limit is **103ps** Maximum but keep as low as possible.
* DDR Traces Length - as short as possible and **8.55” (22cm)** Maximum(UG933)
* VTT resistor **slightly after** the DDR3L RX (and less than a TL length)
* Trace to Trace– spread above the manufacturer limit when space allows.
* DDR differential traces guidelines for **80[ohm]±10%** controlled diff Impedance:
  + See controlled impedance table
* Length matching/Delay matching +-10ps (UG988 table-5-9)
* Via stub Spacing
* Suggested routing layer – layers 6 and 8(8 is preferred due to less stub):

|  |  |
| --- | --- |
| Layer | Type |
| L1 | Signal |
| L2 | GND |
| L3 | POWER |
| L4 | Signal (low speed, PMODS) + Power |
| L5 | GND |
| L6 | Signal (High speed) |
| L7 | GND |
| L8 DDR | Signal (High speed, less Stub) + Power |
| L9 | GND |
| L10 | Signal |

* Layout the following groups with same routing/layout/layer/vias:
  + **ACC\_Group:**
    - Address lines [0-14]
    - BA[0-2]
    - CK\_P, CK\_N, CLKE
    - NCS, RAS,
    - CAS
  + **Data\_Group0 – DDR BL0:**
    - DQ[0-7]
    - DDR\_DM0
    - DDR\_DQS0\_N
    - DDR\_DQS0\_P
  + **Data\_Group1 – DDR BL1:**
    - DQ[8-15]
    - DDR\_DM1
    - DDR\_DQS1\_N
    - DDR\_DQS1\_P
* Note 1 - DQ Only - Bytes groups swapping is optional on the Memory device size.
* Note 2 - DQ Only - bits in Bytes groups swapping is optional on the Memory device size.

**USB and USB PHY**

Route USB to impedance 0f 90 ohm

Impedance calculators

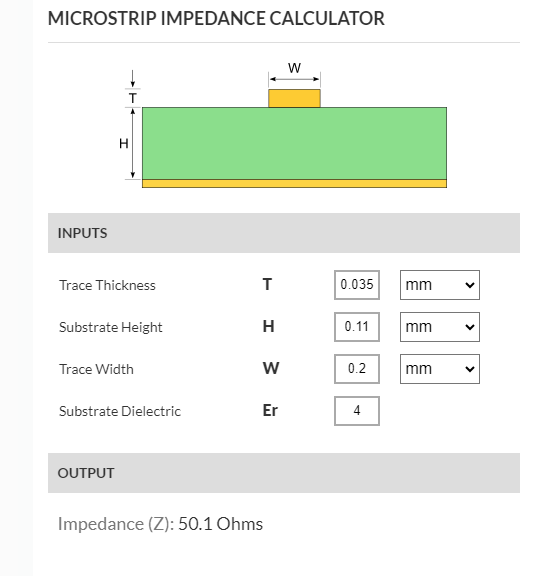
<https://www.pcbway.com/pcb_prototype/impedance_calculator.html>

<https://www.eeweb.com/tools/microstrip/>

**Controlled impedance table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Controlled impedance all units in [mm] | Trace Thickness T | substrate height H | trace width W | Spacing S | Substrate Dielectric Er |
|  |
| 50 ohm SE **microstrip** | 0.035 | 0.11 | 0.2 | - | 4 |  |
| 50 ohm SE **stripline** | 0.035 | 0.11 | TBD | - | 4.29 |  |
| 40 ohm SE microstrip | 0.035 | 0.11 | 0.29 | - | 4 |  |
| 40 ohm SE stripline | 0.035 | 0.11 | TBD | - | 4.29 |  |
|  |  |  |  |  |  |  |
| 80 ohm diff microstrip | 0.035 | 0.11 | 0.13 | 0.2 | 4.9 |  |
| 80 ohm diff Stripline | 0.035 | 0.11 | 0.3 | 0.2 | 4 |  |
|  |  |  |  |  |  |  |
| 90 ohm diff(USB) - microstrip | 0.035 | 0.11 | 0.3 | 0.2 | 4.9 |  |
| 90 ohm diff(USB) - stripline | 0.035 | 0.11 | TBD | TBD | 4.29 |  |
|  |  |  |  |  |  |  |
| 100 ohm diff microstrip | 0.035 | 0.11 | 0.21 | 0.2 | 4.29 |  |
| 100 ohm diff stripline | 0.035 | 0.11 | TBD | TBD | 4.29 |  |

microstrip trace to SE 50ohm:

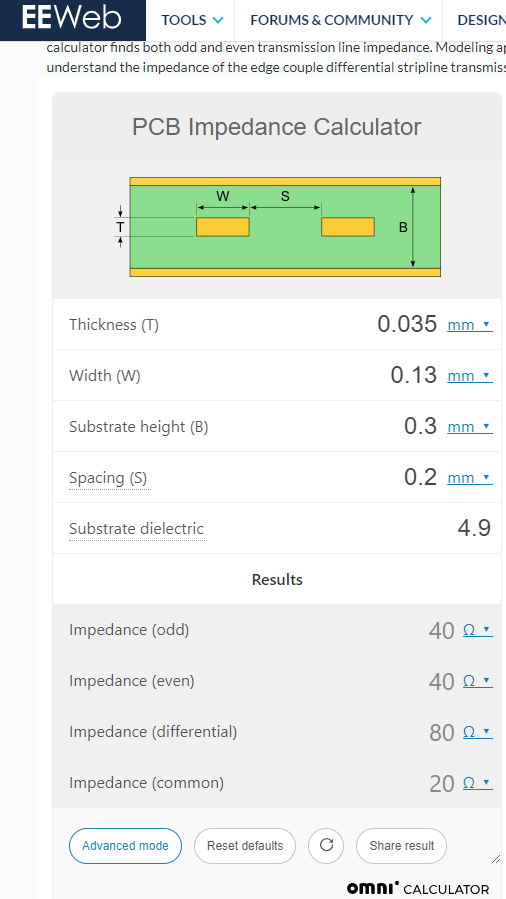


Top trace to SE 40ohm:

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Internal strip line dimensions diff 80 ohms (DDR)

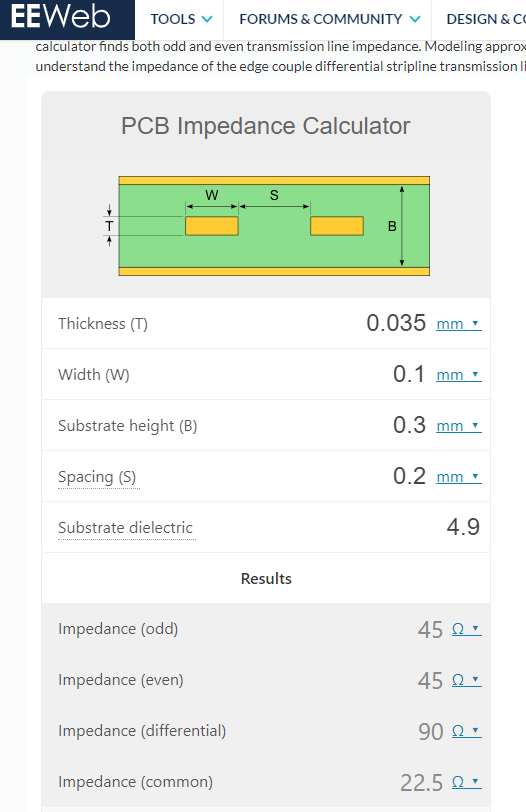


microstrip dimensions diff 80 ohms (DDR)

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Internal strip line dimensions diff 90 ohms (USB)



Differential 100 ohm

